Intel® 82801CAM I/O Controller Hub 3 (ICH3-M)

Specification Update

March 2006

Notice: The 82801CAM product may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Document Number: 290718-010

Contents

Revision History

Revision	Changes	Date
001	Initial Release. Errata 1-15, Specification Change 1, Specification Clarification 1, and Documentation Changes 1-4	July 2001
002	Updates include: •Added Errata 16	September 2001
003	Updates include: •Errata #17-21 •Specification Changes #2-4 •Specification Clarifications #2-7 •Documentation Changes #5-7	November 2001
004	Updates include: •Errata #22-25 •Specification Clarifications #8-14 •Documentation Changes #8-12	March 2002
005	Updates include: •Errata #26-27 •Specification Clarifications #15-23 •Documentation Changes #13-16	July 2002
006	Updates include: •Added Errata #28	August 2003
007	Updates include: •Added Errata #29	December 2003
008	Updates include: •Documentation Change #17	November 2004
009	Updates include: •Added Errata #30-31 •Update Specification Changes #5 •Update Specification Clarification #24	March 2005
010	Updates include: •Added Errata #32-33	April 2006

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents. This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel® 82801CAM I/O Controller Hub 3 (ICH3-M) Datasheet	290716

Nomenclature

Errata are design defects or errors. Errata may cause the ICH3-M's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Component Marking Information

The Intel® 82801CAM I/O Controller Hub 3 (ICH3-M) may be identified by the following component markings:

ICH3-M Stepping	S-Spec	Top Marking	Notes
B0	QB62, QB63	FW82801CAM QB62, QB63	Engineering Sample
B0	SL5LF	FW82801CAM	Production
B1	QC42	FW82801CAM	Engineering Sample
B1	SL5YP	FW82801CAM	Production

Summary Table of Changes

The following tables identify the Specification Changes, Errata, Specification Clarifications, and Documentation Changes that apply to the Intel® 82801CAM I/O Controller Hub 3 Mobile (ICH3-M) product. Intel intends to fix some of the errata in a future stepping of the component(s), and to account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Table

Stepping

X: Specification Change, Erratum, Specification Clarification or Documentation Change that applies to a stepping or to this product line.

(No mark) or
(Blank Box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc: Document change or update that will be implemented.

Fix: This erratum is intended to be fixed in a future stepping of the component.

Fixed: This erratum has been previously fixed.

No Fix: There are no plans to fix this erratum.

Eval: Plans to fix this erratum are under evaluation.

Bar: This item is either new or modified from the previous version of the document.

Other

Shaded: Shaded rows in tables identify items that are new or have been modified since the previous version of this document.

Errata (Sheet 1 of 2)

Erratum Number	B0 Stepping	B1 Stepping	Status	ERRATA
1	X	X	No Fix	IOAPIC and C2/C3
2	X	X	No Fix	AC '97 "Missed Sample"
3	X	X	No Fix	DMA Mode Data Corruption
4	X	X	No Fix	Power-button/CF9 Reset
5	X	X	No Fix	Special Cycle Non-Zero Address
6	X	X	No Fix	LPC Reset Timing Issue
7	X		Fix	USB Subsystem VID Visible When Controllers Are Disabled

Errata (Sheet 2 of 2)

Erratum Number	B0 Stepping	B1 Stepping	Status	ERRATA
8	X	X	No Fix	Unexpected SMI with S1-M
9	X		Fix	S1-M LDRQ# System Hang Issue
10	X	X	No Fix	USB Impedance Compensation Issue
11	X	X	No Fix	AC '97 Link Reset Race Condition
12	X		Fix	LAN µC PCI Protocol Violation
13	X	X	No Fix	SERIRQ and CLKRUN#
14	X	X	No Fix	SM Bus Arbitration Erratum
15	X	X	No Fix	I^2C Read Command Issue
16	X		Fix	STPCLK# Throttling
17	X	X	No Fix	PERR# Response Issue
18	X	X	No Fix	PERR# Detection Issue
19	X	X	No Fix	SE0 Resume Causes Disconnect
20	X	X	No Fix	ATA Rising Edge Slew Rate Issue
21	X	X	No Fix	Master Abort Issue
22	X	X	No Fix	IDE Hang Issue
23	X	X	No Fix	Delayed Transaction Timer Status Bit
24	X	X	No Fix	DWORD I/O Cycle Native Mode IDE Issue
25	X	X	No Fix	SMBus NACK and Process Call
26	X	X	No Fix	AC'97 FIFO Error Bit Software Overrun Issue
27	X	X	No Fix	RTC I/O Read Issue
28	X	X	No Fix	Multi word DMA Mode 1 Issue
29	X	X	No Fix	USB Buffer Overrun Erratum
30	X	X	No Fix	Full-speed USB ISOC End of Packet
31	X	X	No Fix	DPRSLPVR May Not Be Properly Initialized on Cold Boot

Specification Changes

Number	SPECIFICATION CHANGES
1	Changes to DC Characteristics
2	SMBus 2.0 Current Specification
3	USBCLK High and Low Time Change
4	Update to DC Characteristics
5	Update to GPI_ROUT Register

Specification Clarifications

Number	SPECIFICATION CLARIFICATIONS
1	Arbitration ID Register Language
2	Parameter Clarification on PWROK and VGATE Signals
3	S1-M and IOAPIC Clarification
4	SMBus Slave I/F Access
5	Native Mode IDE
6	GPIO[32:43] Note Clarification
7	Intruder Detect Signal
8	RTC Power Status Bit
9	Hub Arbiter Disable (ARB_DIS) Bit
10	V5REF / Vcc3_3 Sequencing Requirements
11	RTC Event Enable Bit
12	USB Run/Stop Bit
13	CPUPWR_FLR Bit
14	Global Standby Timer (GST) Resolution
15	RTC Set Bit
16	12-Clock Retry Enable
17	SMBus Block Transfers and TCO
18	End of SMI Bit
19	SMBus Wake
20	XOR Chain #4 Output and Chain List Clarification
21	USB Legacy Keyboard Mouse Control
22	RTC Voltage
23	LPC LPCPD# Protocol Clarification
24	GPIO Note Change Clarification

Documentation Changes

Number	DOCUMENTATION CHANGES
1	PCI Device Revision ID Table added
2	USB Timing Table
3	LPC Devices and CLKRUN#
4	Global Control Register for the Audio and Modem Functions
5	GPIO[23:16] are not 5V tolerant
6	USB Timing Update: EOP Width
7	Removal of DC Output Enhanced Mode Hublink Characteristics
8	Vcc1_8 Max Power Consumption at S0
9	V5REF_Sus Connectivity
10	SLP_S1# Power State at S3-S5

Documentation Changes

Number	DOCUMENTATION CHANGES
11	SLP_S1# and STP_PCI# signals are swapped in 'S0 to S5 to S0' Timing Diagram
12	LAN_RST# is Inactive after VccLAN Supplies Active
13	SUSCLK AC Timing Specification
14	SUSCLK During PCIRST#
15	USB PORTSC Register
16	TCO Registers
17	Generic Decode Range 2 Register Description Change

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Errata

1. IOAPIC and C2/C3

Problem: Interrupts get missed when C-states and IOAPIC are enabled.

Implication: System clock is observed running slower when C2/C3 and IOAPIC are enabled and IRQ8 is used for system clock update. Result - time lost. This phenomenon is due to a race condition that exists between C2/C3 break events, and the latency of interrupt messages on APIC bus.

Workaround: C2/C3/C4 and IOAPIC cannot be used together. De-feature IOAPIC if using C2/C3/C4.

Note: See Platform Design Guide for recommended implementation of serial IOAPIC bus.

Status: There are no plans to fix this erratum.

2. AC ’97 “Missed Sample”

Problem: If an incoming data overrun occurs on ACLink within a 2 clock time window of an AC ’97 write completion on the hub interface, the AC ’97 controller will not see the FIFOE status bit.

Implication: There is a possibility of missing a single sample of incoming (Modem In, Mic In, or PCM In) AC ’97 data. For audio data, this will be undetectable. For modem, sample overrun could cause a single bit corruption. On these rare instances, SW will request a packet re-transmit as a result of CRC error detection, resulting in a negligible performance hit (modem data packet re-tries occur frequently due to telephone line noise). Neither Audio nor Modem drivers are affected, since they do not implement overrun error handlers. The boundary conditions required for this to occur are extremely unlikely. This issue has been observed only in artificial, highly stressed system test environments.

Workaround: Not required.

Status: There are no plans to fix this erratum.

3. DMA Mode Data Corruption

Problem: DMA compatible mode on the secondary channel causes data corruption on primary channel. If a device on one of the IDE interfaces (e.g., the secondary channel), is operating in Multi-Word DMA Mode with compatible timings where the cycle time is 600 ns, while a device on the other interface (primary channel) is running in PIO mode), the IDE PIO pre-fetch buffer will inadvertently provide an extra piece of secondary channel data to the primary device resulting in data corruption. This happens when DMAREQ is deasserted and a DMA transaction is running while a PIO transaction is outstanding on the other channel.

Implication: Systems configured in this manner may experience a situation in which the DMA IDE controller transfers incorrect data from the PIO configured device. Exactly how this manifests itself in a system is dependent on the system activity at the time.

Workaround: When BIOS is determining which mode(s) an IDE device is capable of, it must not set the DMA capable bits in the ICH3-M if that device only supports Mode-0 DMA or slower. That device should be configured for PIO instead.

Status: There are no plans to fix this erratum.

4. Power-button/CF9 Reset

Problem: If the power-button is pressed (PWRBTN# is asserted) during a CF9 hard reset event (an I/O write of 06h to CF9h), or if a CF9 hard reset sequence is initiated while the power-button is depressed, the ICH3-M will behave as if a power-button override event has occurred and transition the system to S5 state (off).

Implication: The system may unexpectedly transition to the S5 state (turn off). The user will have to awaken the system by pressing the power-button.

Workaround: Software must test the PWRBTN# status bit before attempting a CF9 hard reset; this sequence can reduce the boundary of this issue.

Status: There are no plans to fix this erratum.

5. Special Cycle Non-Zero Address

Problem: Special Cycles immediately followed by any cycle(s) (within 3 hub interface clocks) may result in the ICH3-M driving non-zero data during the address phase of the special cycle. The PCI specification only requires that stable data be driven during the address phase; it does not require that address bits 31:0 be all zeros.

Implication: Non-PCI compliant devices may attempt to claim this special cycle and the device may not function properly. This has only been seen on one PCI graphics card that is no longer produced.

Workaround: None.

Status: There are no plans to fix this erratum.

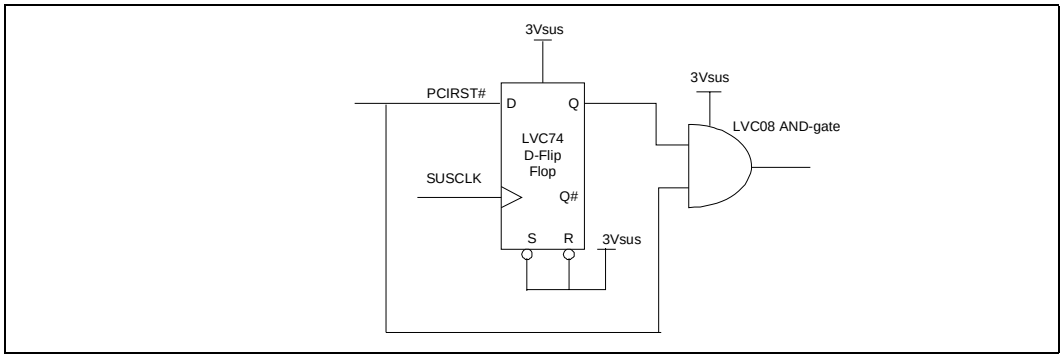
6. LPC Reset Timing Issue

Problem: The ICH3-M specified 1–3 RTC timing of SUS_STAT# inactive to PCIRST# inactive violates the LPC specification of “at least 60 µs.”

Implication: Some LPC devices may not properly reset resulting in failure of the system to boot or resume from a sleep state.

Workaround: Use any one of these three workarounds:

1. Delay PCIRST# by 1 SUSCLK using a D-flop and an AND gate to the LPC devices.



2. Do a CF9 hard reset within the 1st 100 ms of POST.
3. Do not connect the SUS_STAT# to the SIO PD input; instead, implement an external pull-up resistor on the PD input of the SIO.

Status: There are no plans to fix this erratum.

7. USB Subsystem VID Visible When Controllers Are Disabled

Problem: The ICH3-M will respond to reads to Device 29 Function 0 anytime you try to read the Subsystem Vendor ID, even if the function is disabled. The ICH3-M also responds to reads to Device 29 Function 1 if it is disabled and Device 31 Function 1 (IDE) is enabled. Device 29 Function 2 is not affected.

Implication: The expected behavior to any configuration read to a disabled function is “no response” (resulting in a master abort). This issue comes about from the aliasing change in the ICH3-M for SVID between IDE, USB UHCI, and SMBus.

Workaround: None necessary. Testing has shown no OS is affected by this erratum.

Status: Fixed in B1 stepping of ICH3-M.

8. Unexpected SMI with S1-M

Problem: When entering S1-M, peripheral PCI clocks including the PCI clock to the Super IO will be stopped one clock after STP_PCI# is asserted. In the S1-M transition SUS_STAT# is asserted, and in response some SERIRQ agents may drive active low on SERIRQ. The active low may be maintained on the SERIRQ line, as the SERIRQ agents observes SUS_STAT# assertion. The PCI clock to the ICH3-M is stopped later after SLP_S1# is asserted. Since PCI clocks to ICH3-M are still running for some time, the ICH3-M may misinterpret this as a request for an SMI#, INTR, or NMI (depending on which SERIRQ slot is being sampled). Upon exit from S1-M an SMI#, INTR, or NMI may occur in response to this misinterpretation.

Implication: Unexpected INTR, SMI#, or NMI may occur when resuming from S1-Mobile suspend state. System implications will be BIOS/OS dependent. Based on the type of interrupt detected this may result in a system hang.

Workaround: A BIOS workaround has been validated in which SERIRQ must be disabled before entering S1-M state and re-enabled after exiting from S1-M. This will prevent generation of unexpected interrupts. SERIRQ can be disabled by writing a ‘0’ to D31:F0;64h bit-7.

Contact your local Intel Field representative if you require more detailed BIOS workaround information.

Status: There are no plans to fix this erratum.

9. S1-M LDRQ# System Hang Issue

Problem: S1-M transitions in conjunction with LDRQ# assertion may cause a system hang. During a transition to S1-M, the ICH3-M will assert SUS_STAT# low. Some SIOs have been found to drive LDRQ# low in response to SUS_STAT# going low. The ICH3-M should shut off the LDRQ# input buffers when SUS_STAT# is driven low. However, the ICH3-M does not do this, and consequently sends an erroneous DMA transfer.

Implication: A system hang may result if DMA cycles are not suppressed upon entry/exit from S1-M.

After resuming from S1-M, once the DMA unit is enabled to operate, an erroneous DMA transfer may occur which could cause a variety of different failures in the system depending on the attributes of the transfer up to and including data loss and or data corruption.

Workaround: Contact your local Intel Field representative if you require more detailed BIOS workaround information.

Status: Fixed in B1 stepping of ICH3-M.

10. USB Impedance Compensation Issue

Problem: A setup timing issue exists in the ICH3-M's impedance compensation circuit which can cause the USB buffers to shut off, leading to missed USB transmit packets.

Implication: This is likely to result in data loss or may cause data corruption.

Workaround: A BIOS workaround has been validated.

This workaround can only be implemented on ICH3-M B0 silicon marked QB62ES, SL5LF and B1 silicon.

Contact your local Intel Field representative if you require more detailed BIOS workaround information.

Status: There are no plans to fix this erratum.

11. AC '97 Link Reset Race Condition

Problem: If an AC '97 reset is initiated (via GLB_CNT:[1]) just as a new frame is starting, a race condition between AC_RST# asserting and AC_SDIN transitioning from "Ready=1" to ground, due to the reset, may cause an unexpected wake event (SMI) if AC '97 wake events are enabled (via GPE0_EN).

Implication: This will result in an unexpected wake event (SMI) that may not be comprehended by the SMI handler resulting in repeated SMIs.

Workaround: Early in enumeration disable AC '97 wake event and re-enable it after enumeration. BIOS must disable SMI & PME generation when doing a reset to or powering down the codecs. BIOS should clear the related status registers and then re-enable SMI & PME generation.

Status: There are no plans to fix this erratum.

12. LAN µC PCI Protocol Violation

Problem: When the ICH3-M (using an 82562ET/EM) is receiving large files from a peer LAN device using the 10 Mbps data rate, the ICH3-M can cause a system lock-up. Specifically, if the LAN controller has Standby Enable set (EEPROM Word Ah bit-1 = 1), while receiving large files using the 10 Mbps data rate and receives a CU command from the driver after being in Idle state, the ICH3-M will cause a PCI protocol violation within the next few PCI cycles. This will cause the PCI bus to lock-up, further resulting in system hang. This does not occur when the ICH3-M is transmitting large files to another device.

Implication: Large file transfers to the ICH3-M using 10 Mbps can cause the receiving system to lock-up.

Workaround: Clear EEPROM Word Ah bit-1 to 0. The implications of this workaround is an increase power consumption of ~ 40 mW.

Status: Fixed in B1 stepping of ICH3-M.

13. SERIRQ and CLKRUN#

Problem: If Dynamic PCI Clock control is enabled (CLKRUN_EN - Dev 31, Func 0, Offset A0, Bit 2 set to 1), STP_PCI# may be asserted while ICH3-M is driving SERIRQ Start Frame, causing a boundary condition during which ICH3-M may continue to drive a SERIRQ Start Frame for up to two clocks while the external PCICLK to the Super I/O Controller (SIO) may be stopped. If SERIRQ Start

Frame is set to 4 clocks (Start Frame Pulse Width - Dev 31, Func 0, Offset 64h, Bits 1:0 =’00’), the SIO may misinterpret the Start Frame driven from the ICH3-M.

Implication: System hang.

Workaround:

- BIOS should program SERIRQ Start of Frame to either 6 or 8 clocks (Dev 31, Func 0, Offset 64h, Bits 1:0 should be set to ‘01’ or ‘10’).
- Contact your local Intel Field representative if you require more detailed BIOS workaround information.

Status: There are no plans to fix this erratum.

14. SM Bus Arbitration

Problem: ICH3-M will not detect a bus collision when attempting to STOP at the end of a SM Bus transaction as a master. If there is another external Bus Master attempting to access the bus at the same time and wins the arbitration during STOP bit, ICH3-M does not set the Bus Error bit.

Implication: A master attempting a transfer that had actually “lost” may think that its transaction was completed when it was not completed.

Workaround: None.

Status: There are no plans to fix this erratum.

15. I^2C Read Command Issue

Problem: ICH3-M uses HST_D0 register (D31:F3, offset 05h) as the byte count register instead of depending on the LAST_BYTE bit in Host Control register (D31:F3, offset 02h: bit5) to end the transaction.

Implication: The transaction will stop prematurely if HST_D0 contains a number smaller than the intended transaction.

Workaround: No workaround for 10-bit addressing I^2C devices. The SMBus read command for 7-bit addressing may be used with I^2C devices.

Status: There are no plans to fix this erratum. De-feature I^2C read command.

16. STPCLK# Throttling Issue

Problem: Upon exit from a throttling (STPCLK# based) induced C2 transition, the ICH3-M’s internal state machine may improperly sequence. This causes incorrect behavior of GMCH resulting in data not being snooped on the Processor System Bus.

Implication: Snoop cycles on the Processor System Bus are impacted and may cause data incoherency between processor cache and main memory must disable all STPCLK# based throttling.

Workaround: Must disable all STPCLK# based throttling. For systems that have a processor which supports Intel® SpeedStep® Technology, a BIOS workaround has been validated that switches the processor to battery optimized mode when thermal conditions requires throttling.

Refer to the BIOS workaround reference code document

Status: Fixed in B1 stepping of ICH3-M.

17. PERR# Response Issue

Problem: If ICH3-M's Parity Error Response Enable (PER) Bit in Bridge_CNT register (D30:F0, offset 3Eh: bit 0) is disabled (default), it will block PERR# from being asserted when a data Parity Error is detected on the PCI bus during LPC or legacy DMA master read cycles, or when the ICH3-M is the target for write cycles to Device 31 Function 0 and Function 3. This bit should only block PERR# from being asserted when a PCI data Parity Error is detected during PCI-to-memory writes or CPU-to-PCI read cycles.

This issue was found during ongoing internal validation using a synthetic test environment and there have been no failures reported by customers.

Implication: PERR# will not be asserted when the PCI Parity Error is detected during LPC or legacy DMA master read cycles, or when ICH3-M is the target for write cycles to Device 31 Function 0 and Function 3.

Workaround: BIOS needs to set PER of Bridge_CNT when the parity error detection is supported on LPC or legacy DMA.

Status: There are no plans to fix this erratum.

18. PERR# Detection Issue

Problem: ICH3-M's Detected Parity Error (DPE) Bit in SECSTS register (D30:F0, offset 1Eh: bit 15) and PCISTA register (D31:F0, offset 06h: bit 15) will get set when PERR# is asserted by external PCI devices.

This issue was found during ongoing internal validation using a synthetic test environment and there have been no failures reported by customers.

Implication: DPE bit of SECSTS and PCISTA may get erroneously set. These bits are used to report status only. No interrupts will occur.

Workaround: BIOS needs to check DPE bit on all external PCI devices. If PERR# was asserted by external PCI devices, BIOS needs to clear DPE of SECSTS and PCISTA because these bits may get erroneously set.

Status: There are no plans to fix this erratum.

19. SE0 During Resume Causes Disconnect

Problem: A transient SE0 during an upstream resume signal from the USB peripheral to the ICH3-M while the system is in S3/S4 sleep states will cause the ICH3-M to register a disconnect. This violates the USB Rev 1.1 specification.

Implication: The implication is Operating System dependent. It can range from additional latency on a resume before the USB device is functional (after a resume), to the USB device no longer works after a resume - in which case a system reboot must be done to obtain USB device functionality. In all cases the rest of the system does resume

Workaround: None.

Status: There are no plans to fix this erratum.

20. ATA Rising Edge Slew Rate Issue

Problem: ICH3-M's ATA Rising edge slew rate (S_{RISE2}) for DD[15..0] does not meet Ultra ATA/100 Specification.

Implication: Although ICH3-M does not meet S_{RISE2}, ICH3-M does meet the ATA signal integrity guidelines and AC timings. Furthermore, no failures have been reported in system validation or customers to date as a result of this erratum.

Workaround: None.

Status: There are no plans to fix this erratum.

21. Master Abort Mode issue

Problem: ICH3-M Master Abort Mode (BRIDGE_CNT – Bridge Control Register, D30:F0, offset 3E-3Fh, bit 5) is a new function. It was implemented incorrectly. A missing qualification can cause a Target Abort signal to a PCI agent that was uninvolved in the transfer.

Implication: ICH3-M could Target Abort the wrong bus master.

Workaround: De-feature Master Abort Mode. Power on default is Master Abort Mode bit is disabled. BIOS needs to make sure this bit is not enabled.

Status: There are no plans to fix this erratum.

22. IDE Hang Issue

Problem: An arbitration deadlock in the ICH3-M may occur if IDE traffic is combined with heavy graphic traffic and internal/external PCI Bus Master traffic to memory.

Implication: This issue may lockup the IDE bus master causing a system hang. This issue was found during ongoing internal validation using a synthetic test environment and there have been no failures reported by customers.

Workaround: BIOS needs to set configuration register (Device 31, Function 0, offset FCh, bit 23) to prevent the arbitration deadlock. Contact your local Intel Field representative if you require more detailed BIOS workaround information.

Status: There are no plans to fix this erratum.

23. Delayed Transaction Timer Status Bit

Problem: After a delayed transaction has been serviced, the discard timer is not reset which incorrectly times out. This timeout sets the SERR# due to Delayed Transaction Timeout bit (D30:F0:92h:Bit 1). This may result in generation of SERR# based NMIs if the SERR# enable on Delayed Transaction Timeout bit (D30:F0:92h:Bit 1) is set to a ’1’ by software or system BIOS.

Implication: This may cause excessive NMIs to occur which impacts system performance.

Workaround: A BIOS workaround has been identified. Refer to ICH3-M BIOS Specification Update for more details.

Status: There are no plans to fix this erratum.

24. DWORD I/O Cycle Native Mode IDE Issue

Problem: An I/O read crossing a DWORD boundary being sent from processor to the ICH3-M may not complete correctly. The ICH3-M will treat such a transaction as two single DWORD I/O accesses. If native mode IDE addressing is enabled, the ICH3-M will return the first I/O cycle completion request to the MCH but the second I/O cycle may get decoded to the IDE controller instead of its intended address.

Implication: System may hang while processor waits for return of I/O cycle.

Workaround: Disable Native Mode IDE in BIOS. See ICH3-M BIOS Specification Update for more details.

Status: There are no plans to fix this erratum.

25. SMBus NACK and Process Call

Problem: ICH3-M SMBus controller fails to respond after being NACKed on the 4th data phase when using the SMBus command Process Call (with or without I^2C enabled).

Implication: This issue may lockup the SMBus controller and cause the system to stop responding. This issue was found during ongoing internal validation using a synthetic test environment and there have no failures reported by known commercial applications.

Workaround: No workaround.

Status: There are no plans to fix this erratum.

26. AC'97 FIFO Error Bit Software Overrun Issue

Problem: ICH3-M may set the FIFOE Bit in the Input Status Register after software overrun error occurs on a highly stressed system. The ICH3-M should only set the FIFOE bit on a hardware overrun. Bit affected depends on which stream is currently running:

PCM IN - PISR (D31:F5:I/O Offset NABMBAR + 06h:Bit 4)

Microphone IN - MCSR (D31:F5:I/O Offset NABMBAR + 26h:Bit 4)

Modem IN - MISR (D31:F5:I/O Offset MBAR + 06h:Bit 4)

Implication: No data was lost because software did not expect an additional sample. Driver vendors typically do not use this status bit in their production drivers.

Workaround: No workaround.

Status: There are no plans to fix this erratum.

27. RTC I/O Read Issue

Problem: Under certain conditions, a CPU generated I/O read to RTC registers 0-9 may return an incorrect value. The issue occurs on the read path and RTC registers are not impacted. The issue has only been found using a synthetic test environment and has not been reported using commercially available software.

Implication: An operating system which synchronizes the time/date value may get an incorrect value.

Workaround: A BIOS workaround is available. See the ICH3-M BIOS Specification Update for implementation details.

Status: There are no plans to fix this erratum.

28. Multi word DMA Mode 1 Issue

Problem: Data hold time of multi word DMA Mode 1 writes may not meet ATA specification

Implication: No known implication.

Workaround: Program the controller to (Programmed Input/Output) PIO Mode 4 instead.

Status: There are no plans to fix this erratum.

29. USB Buffer Overrun Erratum

Problem: If a USB full-speed isochronous or asynchronous inbound transaction is on the verge of an overrun event (requires 20 us of system latency) and the USB FIFO begins to empty during a 30 ns window immediately prior to the overrun event actually occurring, extra data can be sent to memory. This erratum has only been reproduced with synthetic test environments and not with real world applications.

Implication: Extra data may be sent to memory and/or data could be erroneously written beyond the boundary of the USB buffer allocation. This may result in unpredictable system behaviour. There is no known exposure with real world applications.

Workaround: No workaround.

Status: There are no plans to fix this erratum.

30. Full-speed USB ISOC End of Packet

Problem: If a Full-speed USB ISOC OUT transaction occurs very late in the USB frame such that the payload cannot be contained in that frame, then a bit stuff error is created as defined in the USB 2.0 specification and flagged to both host software and device. When this occurs, and a specific data pattern is present, then the End of Packet (EOP) will not be sent. In this event, devices attached to that UHCI controller may not detect the subsequent Start of Frame (SOF) due to lack of EOP.

Implication: None, the resulting bit stuff error and device not detecting SOF are recoverable events by USB 2.0 system design.

Note: USB ISOC traffic and SOF packets are not necessarily data coherent by definition of the protocol. This issue has only been replicated in a synthetic test environment and has not been reproduced in known system configurations.

Workaround: None

Status: There are no plans to fix this erratum.

31. DPRSLPVR May Not Be Properly Initialized on Cold Boot

Problem: DPRSLPVR signal may not be properly initialized until the ICH3-M core well power rails (Vcc1_5, Vcc3_3) become stable and the ICH3-M receives PCI clock.

Implication: System may fail to boot depending on the power sequencing logic implementation and CPU VR solution used on the platform. Observing the failure is platform design dependent; not all systems are susceptible to this erratum.

Workaround: An external weak pull-down resistor of 100K ohm will ensure DPRSLPVR does not float on affected systems.

Status: There are no plans to fix this erratum.

32. PCI Non-Linear Addressing

Problem: If a PCI Memory Read Multiple or Memory Read Line transaction falls at the last DW of a 32B cache line boundary and non-linear addressing (cache-line wrap mode) is used, the ICH3-M will

pre-fetch data past the cache line boundary. All subsequent PCI bus master reads will get incorrect data. Subsequent CPU cycles to PCI/LPC will get blocked behind the surplus data resulting in a system hang.

Implication: System hang only seen in synthetic test environment. No known commercial PCI devices support cache-line wrap mode using Memory Read Multiple or Memory Read Line

Workaround: None.

Status: No fix.

33. LPC Starvation

Problem: Latency issues on LPC may occur if a PCI bus master is performing large upstream burst to memory and no other PCI devices are requesting the bus. If an LPC cycle occurs during an upstream PCI burst, the completion of the LPC cycle may get delayed until the PCI device completes its transaction and de-asserts its REQ#.

Implication: Under certain operating conditions, latency on the LPC bus may cause delays in accessing data from an LPC based device.

Workaround: None.

Status: No Fix.

Specification Changes

1. Changes to DC Characteristics

Issue: In Section 16.3, *D. C. Characteristics*, replace Table 16-2 with the following table. Shading indicates information that has changed.

Symbol	Associated Signals[2]
V_{IH1}/V_{IL1} (5V Tolerant)	**PCI Signals:** AD[31:0], C/BE[3:0]#, DEVSEL#, FRAME#, IRDY#, TRDY#, STOP#, PAR, PERR#, PLOCK#, SERR#, REQ[4:0]# **PC/PCI Signals:** REQ[A]#/GPIO[0], REQB[#]/REQ[5]#/GPIO[1] **IDE Signals:** PDD[15:0], SDD[15:0], PDDREQ, PIORDY, SDDREQ, SIORDY **Interrupt Signals:** IRQ[15:14], PIRQ[D:A]#, PIRQ[H:E]#/GPIO[5:2] **Legacy Signals:** RCIN#, A20GATE **GPIO Signals:** GPIO[7] **Power Management Signals**: AGPBUSY# (in Mobile)
V_{IH2}/V_{IL2}	**Clock Signals:** CLK66, CLK48, CLK14
V_{IH3}/V_{IL3}	**Interrupt Signals:** SERIRQ **LPC/FWH Signals:** LDRQ[1:0]#, LAD[3:0]/FWH[3:0]; LFRAME#/FWH[4] **Power Management Signals:**BATLOW#, CLKRUN#, PME#, PWRBTN#, RI#, LAN_RST#, RTCRST#, THRM#, VRMPWRGD#/VGATE **System Management Signals:** SMBALERT#/GPIO[11] **EEPROM Signals:** EE_DIN **GPIO Signals:**
V_{IH4}/V_{IL4}	**Clock Signals:** APICCLK
V_{IH5}/V_{IL5}	**SMBus Signals: SMBCLK, SMBDATA** **System Management Signals: INTRUDER#, SMLINK[1:0]** **Power Management Signals: RSMRST#, PWROK** **GPIO Signals: GPIO[28:27]**
V_{IL6}/V_{IH6}	**LAN Signals:** LAN_RXD[2:0]
V_{IL7}/V_{IH7}	**Processor Signals:** FERR#, APICD[1:0]
V_{IL8}/V_{IH8}	**Hub Interface Signals:** HI[11:0], HI_STB#, HI_STB
V_{IL9}/V_{IH9}	**Real Time Clock Signals:** RTCX1
V_{IL10}/V_{IH10} (5 V Tolerant)	**USB Signals:** OC[5:0]#
V_{IL11}/V_{IH11}	**AC '97 Signals:** AC_BITCLK, AC_SDIN[1:0], AC_SYNC **GPIO Signals:**
V_{IL12}/V_{IH12}	**Clock Signals:** LAN_CLK
V_{IL13}/V_{IH13}	**Clock Signals:** PCICLK
V_{DI} / V_{CM} / V_{SE}	**USB Signals:** USBP[5:0][P,N]

Issue: At the end of the above table add note #2 with the following:

Note: 2. To determine signal's power plane, see Table 3-5

Issue: In Section 16.3, *D. C. Characteristics*, replace Table 16-3 with the following table. Shading indicates information that has changed.

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	-0.5	0.8	V	
V_{IH1}	Input High Voltage	2.0	V5REF + 0.5	V	
V_{IL2}	Input Low Voltage	-0.5	0.8	V	
V_{IH2}	Input High Voltage	2.0	Vcc3_3 + 0.5	V	
V_{IL3}	Input Low Voltage	-0.5	0.3Vcc3_3	V	
V_{IH3}	Input High Voltage	0.5Vcc3_3	Vcc3_3 + 0.5	V	
V_{IL4}	Input Low Voltage	-0.5	0.7	V	
V_{IH4}	Input High Voltage	1.7	2.625	V	
V_{IL5}	Input Low Voltage	-0.5	0.6	V	
V_{IH5}	Input High Voltage	2.1	VccSus3_3 + 0.5	V	
V_{IL6}	Input Low Voltage	-0.5	0.3Vcc3_3	V	
V_{IH6}	Input High Voltage	0.6Vcc3_3	Vcc3_3 + 0.5	V	
V_{IL7}	Input Low Voltage	-0.5	0.6	V	
V_{IH7}	Input High Voltage	1.2	Vcc3_3 + 0.5	V	
V_{IL8}	Input Low Voltage	-0.5	HIREF - 0.15	V	Normal Mode
V_{IH8}	Input High Voltage	HIREF + 0.15	Vcc1_8 + 0.5	V	Normal Mode
V_{IL9}	Input Low Voltage	-0.5	0.10	V	
V_{IH9}	Input High Voltage	0.40	2.0	V	
V_{IL10}	Input Low Voltage	-0.5	0.8	V	
V_{IH10}	Input High Voltage	2.0	V5REF_SUS + 0.5	V	
V_{IL11}	Input Low Voltage	-0.5	0.35Vcc3_3	V	
V_{IH11}	Input High Voltage	0.65Vcc3_3	Vcc3_3 + 0.5	V	
V_{IL12}	Input Low Voltage	-0.5	0.3Vcc3_3	V	
V_{IH12}	Input High Voltage	0.6Vcc3_3	Vcc3_3 + 0.5	V	
V_{IL13}	Input Low Voltage	-0.5	0.3Vcc3_3	V	
V_{IH13}	Input High Voltage	0.5Vcc3_3	Vcc3_3 + 0.5	V	
V_{DI}	Differential Input Sensitivity	0.2		V	Note 1
V_{CM}	Differential Common Mode Range	0.8	2.5	V	Note 2
V_{SE}	Single-Ended Receiver Threshold	0.8	2.0	V	

2. SMBus 2.0 Current Specification

Issue: In Table 16-5, replace the V_{OL5} row with the following row:

Symbol	Parameter	Min	Max	Unit	I_{OL}/I_{OH}	Notes
VOL5	Output Low Voltage		0.4	V	4mA	

3. USBCLK High and Low Time Change

Issue: In Table 16-7, replace t10 and t11 rows with the following two rows:

Sym	Parameter	Min	Max	Unit	Notes	Figure
t10	High time	8		ns		16-1
t11	Low time	8		ns		16-1

4. Update to DC Characteristics

Issue: This update replaces Specification Change number 1 and replaces Section 16.3 (D. C. Characteristics), Table 16-2 with the following table. IDE signals were removed from V_{IH1}/V_{IL1} group and added to V_{IH14}/V_{IL14}. Shading indicates information that has changed.

Symbol	Associated Signals[2]
VIH1/VIL1 (5V Tolerant)	**PCI Signals:** AD[31:0], C/BE[3:0]#, DEVSEL#, FRAME#, IRDY#, TRDY#, STOP#, PAR, PERR#, PLOCK#, SERR#, REQ[4:0]# **PC/PCI Signals:** REQ[A]#/GPIO[0], REQB[#]/REQ[5]#/GPIO[1] **Interrupt Signals:** IRQ[15:14], PIRQ[D:A]#, PIRQ[H:E]#/GPIO[5:2] **Legacy Signals:** RCIN#, A20GATE **GPIO Signals:** GPIO[7] **Power Management Signals**: AGPBUSY#
VIH2/VIL2	**Clock Signals:** CLK66, CLK48, CLK14
VIH3/VIL3	**Interrupt Signals:** SERIRQ **LPC/FWH Signals:** LDRQ[1:0]#, LAD[3:0]/FWH[3:0]; LFRAME#/FWH[4] **Power Management Signals:** PME#, PWRBTN#, RI#, LAN_RST#, RTCRST#, THRM#, VRMPWRGD in Server. BATLOW#, CLKRUN#, PME#, PWRBTN#, RI#, LAN_RST#, RTCRST#, THRM#, VGATE **System Management Signals:** SMBALERT#/GPIO[11] **EEPROM Signals:** EE_DIN **GPIO Signals:** GPIO[25,13:12, 8]
VIH4/VIL4	**Clock Signals:** APICCLK
VIH5/VIL5	**SMBus Signals:** SMBCLK, SMBDATA **System Management Signals:** INTRUDER#, SMLINK[1:0] **Power Management Signals:** RSMRST#, PWROK **GPIO Signals:** GPIO[28:27]
VIL6/VIH6	**LAN Signals:** LAN_RXD[2:0]
VIL7/VIH7	**Processor Signals:** FERR#, APICD[1:0]
VIL8/VIH8	**Hub Interface Signals:** HI[11:0], HI_STB#, HI_STB
VIL9/VIH9	**Real Time Clock Signals:** RTCX1
VIL10/VIH10 (5 V Tolerant)	**USB Signals:** OC[5:0]#
VIL11/VIH11	**AC'97 Signals:** AC_BITCLK, AC_SDIN[1:0], AC_SYNC **GPIO Signals:** GPIO[43:32]
VIL12/VIH12	**Clock Signals:** LAN_CLK
VIL13/VIH13	**Clock Signals:** PCICLK
VIL14/VIH14	**IDE Signals:** PDD[15:0], SDD[15:0], PDDREQ, PIORDY, SDDREQ, SIORDY
VDI / VCM / VSE	**USB Signals:** USBP[5:0][P,N]

Issue: At the end of the above table add note #2 with the following:

Note: 2. In order to determine signal's power plane, see Table 3-5

Issue: In Section 16.3, *D. C. Characteristic*s, replace Table 16-3 with the following table. Shading indicates information that has changed.

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	-0.5	0.8	V	
V_{IH1}	Input High Voltage	2.0	V5REF + 0.5	V	
V_{IL2}	Input Low Voltage	-0.5	0.8	V	
V_{IH2}	Input High Voltage	2.0	Vcc3_3 + 0.5	V	
V_{IL3}	Input Low Voltage	-0.5	0.3Vcc3_3	V	
V_{IH3}	Input High Voltage	0.5Vcc3_3	Vcc3_3 + 0.5	V	
V_{IL4}	Input Low Voltage	-0.5	0.7	V	
V_{IH4}	Input High Voltage	1.7	2.625	V	
V_{IL5}	Input Low Voltage	-0.5	0.6	V	
V_{IH5}	Input High Voltage	2.1	VccSus3_3 + 0.5	V	
V_{IL6}	Input Low Voltage	-0.5	0.3Vcc3_3	V	
V_{IH6}	Input High Voltage	0.6Vcc3_3	Vcc3_3 + 0.5	V	
V_{IL7}	Input Low Voltage	-0.5	0.6	V	
V_{IH7}	Input High Voltage	1.2	Vcc3_3 + 0.5	V	
V_{IL8}	Input Low Voltage	-0.5	HIREF - 0.15	V	Normal Mode
V_{IH8}	Input High Voltage	HIREF + 0.15	Vcc1_8 + 0.5	V	Normal Mode
V_{IL9}	Input Low Voltage	-0.5	0.10	V	
V_{IH9}	Input High Voltage	0.40	2.0	V	
V_{IL10}	Input Low Voltage	-0.5	0.8	V	
V_{IH10}	Input High Voltage	2.0	V5REF_SUS + 0.5	V	
V_{IL11}	Input Low Voltage	-0.5	0.35Vcc3_3	V	
V_{IH11}	Input High Voltage	0.65Vcc3_3	Vcc3_3 + 0.5	V	
V_{IL12}	Input Low Voltage	-0.5	0.3Vcc3_3	V	
V_{IH12}	Input High Voltage	0.6Vcc3_3	Vcc3_3 + 0.5	V	
V_{IL13}	Input Low Voltage	-0.5	0.3Vcc3_3	V	
V_{IH13}	Input High Voltage	0.5Vcc3_3	Vcc3_3 + 0.5	V	
V_{IL14}	Input Low Voltage		0.8	V	Note 3
V_{IH14}	Input High Voltage	2.0	V5REF + 0.5	V	
V_{DI}	Differential Input Sensitivity	0.2		V	Note 1
V_{CM}	Differential Common Mode Range	0.8	2.5	V	Note 2
V_{SE}	Single-Ended Receiver Threshold	0.8	2.0	V	

Issue: Add the following Note 3 to Table 16-3:

Note: 3.) These voltages represent steady state values. For transient values, consult V_{RING} in Table 16-6.

Issue: In Table 16-6, *Other DC Characteristics*, add the following row after V_{SE}

Symbol	Parameter	Min	Max	Unit	Notes
V_{RING}	Voltage at Recipient Connector	-1.0	6.0	V	

5. Update to GPI_ROUT Register

Issue: In Section 9.8.1.5, *GPI_ROUT—GPI Routing Control Register (PM—D31:F0)*, replace Table 9.1.8.5 with the following table. Highlighted text in red indicates change.

Bit	Description
31:30	**GPI[15] Route**—R/W. See bits 1:0 for description.
Same pattern for GPI[14] through GPI[3]	
5:4	**GPI[2] Route**—R/W. See bits 1:0 for description.
3:2	**GPI[1] Route**—R/W. See bits 1:0 for description.
1:0	**GPI[0] Route**—R/W. GPIO[15:0] can be routed to cause an SMI or SCI when the GPI[n]_STS bit is set. If the GPIO is not set to an input, this field has no effect. If the system is in an S1–S5 state and if the GPE1_EN bit is also set, then the GPI can cause a Wake event, even if the GPI is NOT routed to cause an SMI# or SCI. 00 = No effect. 01 = SMI# (if corresponding GPE1_EN bit is also set). 10 = SCI (if corresponding GPE1_EN bit is also set). 11 = Reserved. Software must set this bit field to generate the appropriate type of system interrupt, depending on how the SCI_EN bit is set. For example, if the SCI_EN bit is set, then this field must be programmed to 00b or 10b. If the SCI_EN bit is cleared, then this field must be programmed to 00b or 01b. Software must also update this field if the SCI_EN bit is changed.

Note: GPIOs that are not implemented will not have the corresponding bits implemented in this register.

Specification Clarifications

1. Arbitration ID Register Language

Issue: In Section 9.5.8, *Arbitration ID Register*, clarify the operation of this register is for APIC Serial bus mode only. Replace the first sentence with the following:

"This register contains the bus arbitration priority for the APIC serial bus."

Add the following note after the first paragraph:

Note: The Arbitration ID Register can only be written when the APIC clock is running.

2. Parameter Clarification on PWROK and VGATE signals

Issue: The parameter of t177 in Table 16-18 needs to change to "PWROK and VGATE both active to SUS_STAT# inactive".

3. S1-M and IOAPIC Clarification

Issue: In Section 5.12.8.2 Initiating Sleep State, Table 5-40 Sleep Types, the following Note should be added on the Comment of S1 Mobile:

Note: ICH3-M requires that the I/O APIC interrupts be masked before entering S1-M. If software does not mask all interrupts in I/O APIC prior to entering S1-M, the system may hang during resume from S1-M.

4. SMBus Slave I/F Access

Issue: When an external micro-controller accesses the SMBus Slave Interface over the SMLink a translation in the address is needed to accommodate the least significant bit used for read/write control. For example, if the ICH3-M slave address (RCV_SLVA) is left at 44h (default), the external microcontroller would use an address of 88h/89h (write/read).

5. Native Mode IDE

Issue: In Section 10.1.3 remove the following note below the table. The native mode functionality of the controllers are independent of each other.

Note: This register can not be programmed to allow legacy mode on one controller and native on the other. They can only both be set to legacy mode or native mode.

6. GPIO[32:43] Note Clarification

Issue: In Table 9-12, Summary of GPIO Implementation, replace the GPIO[32:43] with the following row:

GPIO	Type	Alternate Function (Note 1)	Power Well	Notes
GPIO[32:43]	I/O	Unmuxed	Core	Input active status read from **GP_LVL2** register bits[32:43]. Output controlled via **GP_LVL2** register bits [32:43]

7. Intruder Detect Signal

Issue: Add to the following paragraph to Section 5.13.1.2

Once the INTRUDER# signal goes active, the INTRD_DET bit gets set. The bit will remain set even after the INTRUDER# input goes inactive and if software hasn't tried to clear it. There is a recovery time up to 65 microseconds on the INTRD_DET bit. The bit may not get cleared for up to 65 microseconds after software has issued a write '1' to clear the INTRD_DET bit. Software will not be able to clear the bit as long as INTRUDER# signal is active as setting the bit has priority over the software clear.

8. RTC Power Status Bit

Issue: In Section 9.8.1.3, *GEN_PMCON_3--General PM Configuration 3 Register,* replace bit 2 description with the following:

2	**RTC Power Status (RTC_PWR_STS)**—R/WC. 0 = Software clears this bit by writing a 0 to the bit position. 1 = Indicates that the RTC battery was removed or has 0 volts. This bit is set when RTCRST# signal is low. **NOTE:** Clearing CMOS in an ICH3-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.

9. Hub Arbiter Disable (ARB_DIS) Bit

Issue: Add the following note to *PM2_CNT--Power Management 2 Control Register, Bit 0*, in Section 9.8.3.9:

0	**Arbiter Disable (ARB_DIS)**—R/W. 0 = Enable Hub Interface arbiter. 1 = Disable Hub Interface arbiter. ARB_DIS will only disable the arbiter at the Hub Interface to prevent up-bound traffic. Consequently, the PCI arbiter will continue to issue GNT#s even when ARB_DIS is set. Note that after the arbiter is disabled, the Processor must not initiate any down-bound reads to PCI devices that may have up-bound posted data, as this will result in system deadlock. **Note:** In general, software should not attempt any non-posted accesses during arbiter disable except to the ICH3-M's power management registers. This implies that interrupt for any unmasked hardware interrupts and SMI/NMI should check ARB_DIS status before reading from ICH3-M devices.

10. V5REF / Vcc3_3 Sequencing Requirements

Issue: In Section 2.20.3, *V5REF / Vcc3_3 Sequencing Requirements*, replace the first paragraph with the following:

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH3-M. V5REF must be powered up before V_{CC3_3}, or after V_{CC3_3} within 0.7 V. Also, V5REF must power down after V_{CC3_3}, or before V_{CC3_3} within 0.7 V. The rule must be followed in order to ensure the safety of the ICH3-M. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the V_{CC3_3} rail. Figure 2-3 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

This rule also applies to the standby rails, but in most platforms, the V_{CCSUS3_3} rail is derived from the V_{CCSUS5} and therefore, the V_{CCSUS3_3} rail will always come up after the V_{CCSUS5} rail. As a result, V_{5REF_SUS} will always be powered up before V_{CCSUS3_3}. In platforms that do not derive the V_{CCSUS3_3} rail from the V_{CCSUS5} rail, this rule must be comprehended in the platform design.

11. RTC Event Enable Bit

Issue: In Section 9.8.3.2, *PM1_EN--Power Management 1 Enable Register*, change the Power Well bit description to the following:

Power Well:	Bits 0-7:	Core
	Bits 8, 9:	Resume
	Bit 10:	RTC
	Bits 11-15:	Resume

12. USB Run/Stop Bit

Issue: Add the following note to the USBCMD--USB Command Register, Bit 0, in Section 11.2.1:

Note: The USB run/stop bit should be cleared only under one of the following conditions:

1. There are no transaction descriptors in the schedule.
2. A reset of the USB host controller is guaranteed prior to a subsequent run/stop bit assertion.

13. CPUPWR_FLR Bit

Issue: In Section 9.8.1.2, *GEN_PMCON_2--General PM Configuration 2 Register*, replace bit 1 description with the following:

1	**CPU Power Failure (CPUPWR_FLR)**—R/WC. 0 = Software clears this bit by writing a **'0'** to the bit position. 1 = Indicates that the VGATE signal from the processor's VRM went low. This bit will not be set if VGATE went low due to a Intel® SpeedStep™ technology transition, during C4 entry/exit, or S1-M entry/exit (if DPSLP# is enabled).

14. Global Standby Timer Accuracy

Issue: Add the following note to Section 9.8.1.1, *GEN_PMCON_1--General PM Configuration 1 Register*:

Note: The Global Standby Timer (GST) has a timeout resolution of approximately 1 minute (+/- seconds).

15. RTC SET Bit

Issue: The SET Bit (bit-7) in RTC_REGB should be set then cleared early in BIOS POST after each powerup directly after coin-cell battery insertion.

16. 12-Clock Retry Enable

Issue: The description for the 12-Clock Retry Enable Bit (bit-1) in Device 30:F0;CNF (50h) register is incorrect. There is no relationship to PCI locked cycles. The description is changed accordingly as indicated:

12-Clock Retry Enable - R/W, system BIOS must set this bit for PCI compliance.

1 = ICH3-M will retry a PCI to memory cycle (read or write) if the ICH3-M is not able to complete the transfer in 12 PCI clocks.

0 = ICH3-M will insert as many wait states as needed to complete the PCI to memory cycle.

17. SMBus Block Transfers and TCO

Issue: The BIOS should always clear the SECOND_TO_STS bit (TCO2_STS register, TCOBase+06h, bit-1) before executing any SMBus Block Reads or Writes.

18. End of SMI Bit

Issue: In Section 9.8.3.14 (SMI_EN) add the following note to bit-1:

Note: ICH3-M is able to generate 1st SMI after reset even though EOS bit is not set. Subsequent SMI's require EOS bit is set.

19. SMBus Wake

Issue: In Table 5-40 *Causes of Wake Events*, replace the SMBALERT# with the following row:

Cause	States Can Wake From	How Enabled
SMBALERT#	S1-S5	Always enabled as a wake event

In Section 5.17.5, first paragraph, S4 is changed to S5.

In Section 9.8.3.10 GPE0_STS - General Purpose Event 0 Status Register, add the following note to bit-7:

Note: The SMBALERT_STS bit (D31:F3:I/O Offset 00h:bit-5) should be cleared by software before this bit is cleared.

20. XOR Chain #4 Outputs and Chain List Clarification

Issue: Table 18-6 XOR Chain #4 is made up of two independent XOR chains with two independent outputs. The first chain starts at SDD8 and ends with the output GPIO8. The second chain starts at PME# and ends with the output BATLOW#. Replace Table 18-6 with corrected table sequence below:

Table 18-6. XOR Chain #4 (RTCRST# Asserted for 7 PCI Clocks While PWROK Active)

Pin Name	Ball #	Notes
SDD8	W13	Top of 1st XOR Chain
SDD6	AA13	2nd signal in XOR
SDD5	Y14	
SDD7	W15	
SDD10	Y15	
SDD11	AC16	
SDD3	AB16	
SDD9	Y16	
SDD12	AB17	
~~SDD15~~ SDD2	~~AC18~~ AC17	
SDD4	W16	
~~SDIOW#~~ SDD13	~~AA18~~ AA17	
~~SDD2~~ SDD15	~~AC17~~ AC18	
SDD0	Y17	
SDDREQ	AB18	
SDD14	Y18	
~~SDD13~~ SDIOW#	~~AA17~~ AA18	
SDD1	W17	
SIORDY	AB19	
SDIOR#	AC19	
SDDACK#	Y19	
SDA1	AA19	
SDA2	AB20	

Pin Name	Ball #	Notes
OC0#	E12	Last in the 1st XOR Chain
GPIO8	**W2**	**1st OUTPUT**
PME#	W1	Top of 2nd XOR Chain in XOR #4
GPIO25	W3	2nd signal in XOR
PCIRST#	Y1	
GPIO13	Y2	
GPIO28	Y3	
GPIO12	Y4	
SLP_S5#	AA2	
GPIO27	W4	
SMLINK1	AB2	
PWRBTN#	AB1	
CLKRUN#	AC2	
SMLINK0	AC3	
SUSCLK	AA4	
SUS_STAT#	AB4	
SMBCLK	AC4	
SLP_S3#	AA5	
SMBDATA	AB5	
SMBALERT#/GPIO11	AC5	
OC4#	A12	
OC3#	B12	
OC2#	C12	

Pin Name	Ball #	Notes
SDA0	AC20	
SDCS3#	AC22	
SDCS1#	AC21	
HI7	T23	
HI11	R19	
HI6	R20	
HI5	R22	
HI9	P19	
HI4	P21	
HI_STB	N22	
HI10	N19	
HI3	N20	
HI8	M19	
HI1	M21	
HI2	M23	
HI0	L22	
HICOMP	K19	
APICD0	J20	
APICD1	J21	
FERR#	J22	
SERIRQ	H22	
GPIO38	H21	
SPKR	H23	
GPIO41	G21	
GPIO39	G23	
GPIO40	F23	
GPIO43	E23	
GPIO42	D23	

Pin Name	Ball #	Notes
OC1#	D12	
OC5#	A11	
~~AC_SDIN0~~	~~B11~~	Not in chain
AC_RST#	D11	
USBP0P	D19	
USBP0N	D18	
USBP1P	A19	
USBP1N	A18	
USBP2P	E17	
USBP2N	E16	
USBP3P	B17	
USBP3N	B16	
USBP4P	D15	
USBP4N	D14	
USBP5P	A15	
USBP5N	A14	
LAN_TXD2	A10	
LAN_TXD1	C10	
EE_SHCLK	D10	
LAN_RXD2	A9	
LAN_TXD0	B9	
EE_CS	E9	
LAN_RXD1	A8	
LAN_RXD0	C8	
EE_DIN	D8	
EE_DOUT	E8	
LAN_RSTSYNC	D7	Last in the 2nd XOR Chain
BATLOW#	**AB3**	**2nd OUTPUT**

21. USB Legacy Keyboard Mouse Control

Issue: • In Section 11.1.16 (USB_LEGKEY) add the following note to bits [15, 11:8, 6]:

Note: This bit reports same value in all USB UHCI controllers.

• In Section 11.1.16 (USB_LEGKEY) and the following note to bits [7, 5, 3:0]:

Note: Setting this bit in any controller enables the function.

22. RTC Voltage

Issue: In Table 16-6 - *Other DC Characteristics*, replace VccRTC with the following:

Symbol	Parameter	Min	Max	Unit	Notes
Vcc(RTC)	Powered by Coin Cell Battery	2.0	3.3	V	
	Powered by Power Supply	2.0	3.6	V	

23. LPC LPCPD# Protocol Clarification

Issue: The LPC specification defines the LPCPD# protocol where there is at least 30uS from LPCPD# assertion to LRST# assertion. This specification explicitly states that this protocol only applies to entry/exit of low power states which does not include asynchronous reset events. The ICH3-M will assert both SUS_STAT# (connects to LPCPD#) and PCIRST# (connects to LRST#) at the same time when the core logic is reset (via CF9, PWROK, etc). This is not inconsistent with the LPC LPCPD# protocol.

24. GPIO Note Change Clarification

Issue: Note 1 of Table 9-12 (Summary of GPIO Implementation) should read as follows:

All GPIOs default to their alternate function and therefore may be subject to further design constraints.

Documentation Changes

1. PCI Device Revision ID Table Added

PCI Revision ID Register values (PCI offset 08h) for all ICH3-M functions are listed in the following table.

This information is not listed in the datasheet. This is the standard reference document for all Revision ID values.

Device, Function	Description	Intel® ICH3-M B0 Rev ID
D8, F0	LAN	41h
D29, F0	USB Controller 1	01h
D29, F1	USB Controller 2	01h
D29, F2	USB Controller 3	01h
D30, F0	P2P Bridge	41h
D31, F0	P2L Bridge	01h
D31, F1	IDE	01h
D31, F3	SMBus	01h
D31, F5	AC '97 Audio	01h
D31, F6	AC '97 Modem	01h

NOTES:

1. From a software perspective, the integrated LAN Controller (D8:F0) appears to reside on the secondary side of the ICH3-M virtual PCI-to-PCI Bridge. This is typically Bus 1, but may be assigned a different number, depending upon system configuration.
2. The ICH3-M integrated LAN Controller (D8:F0) provides support for configurable Subsystem ID and Subsystem Vendor ID fields. After reset, the LAN Controller automatically reads addresses Ah through Ch of the EEPROM. The LAN Controller checks bits 15:13 in the EEPROM word Ah.

2. USB Timing Table

Issue: In Section 16.4, *AC Characteristics*, replace Table 16-12 with the following table. Shading indicates information that has changed.

Sym	Parameter	Min	Max	Units	Notes	Fig
Full Speed Source (Note 7)						
t100	USBPx+, USBPx- Driver Rise Time	4	20	ns	1, C_L = 50 pF	16-13
t101	USBPx+, USBPx- Driver Fall Time	4	20	ns	1, C_L = 50 pF	16-13
t102	Source Differential Driver Jitter To Next Transition For Paired Transitions	 -3.5 -4	 3.5 4	 ns ns	2, 3	16-14
t103	Source SE0 interval of EOP	160	175	ns	4	16-15
t104	Source Jitter for Differential Transition to SE0 Transition	-2	5	ns	5	
t105	Receiver Data Jitter Tolerance To Next Transition For Paired Transitions	 -18.5 -9	 18.5 9	 ns ns	3	16-14
t106	EOP Width: Must accept as EOP	85		ns	4	16-15
t107	Width of SE0 interval during differential transition		14	ns		
Low Speed Source (Note 8)						
t108	USBPx+, USBPx- Driver Rise Time	75	300	ns ns	1, 6 C_L = 50 pF C_L = 350 pF	16-13
t109	USBPx+, USBPx- Driver Fall Time	75	300	ns ns	1,6 C_L = 50 pF C_L = 350 pF	16-13
t110	Source Differential Driver Jitter To Next Transition For Paired Transitions	 -25 -14	 25 14	 ns ns	2, 3	16-14
t111	Source SE0 interval of EOP	1.25	1.50	µs	4	16-15
t112	Source Jitter for Differential Transition to SE0 Transition	-40	100	ns	5	
t113	Receiver Data Jitter Tolerance To Next Transition For Paired Transitions	 -152 -200	 152 200	 ns ns	3	16-14
t114	EOP Width: Must accept as EOP	670		ns	4	16-15
t115	Width of SE0 interval during differential transition		210	ns		

3. LPC Devices and CLKRUN#

Issue: In Section 5.12.7.6, *LPC Devices and CLKRUN#*, add the following information:

The LDRQ# inputs are ignored by the ICH3-M when the PCI clock is stopped to the LPC devices to avoid misinterpreting the request. The ICH3-M assumes that only one more rising PCI clock edge occurs at the LPC device after the assertion of STP_PCI#. Upon deassertion of STP_PCI#, the ICH3-M assumes that the LPC device receives its first clock rising edge corresponding to the ICH3-M's second PCI clock rising edge after the deassertion.

4. Global Control Register for the Audio and Modem Functions

Issue: In Section 13.2.8, *GLOB_CNT—Global Control Register*, replace the row for bit 1 with the following:

1	**AC '97 Cold Reset#**—R/W. 0 = Writing a "0" to this bit causes a cold reset to occur throughout the AC '97 circuitry. All data in the controller and the codec will be lost. Software needs to clear this bit no sooner than the minimum number of ms have elapsed. 1 = This bit defaults to 0; hence, after reset, the driver needs to set this bit to a 1.

Issue: In Section 14.2.8, *GLOB_CNT—Global Control Register*, replace the row for bit 1 with the following:

1	**AC '97 Cold Reset#**—R/W. 0 = Writing a "0" to this bit causes a cold reset to occur throughout the AC '97 circuitry. All data in the controller and the codec will be lost. Software needs to clear this bit no sooner than the minimum number of ms have elapsed. 1 = This bit defaults to 0; hence after reset, the driver needs to set this bit to a 1.

5. GPIO [23:16] are not 5V tolerant

Issue: In Section 2.18, General Purpose I/O, the note below the table should be replaced with:

Only GPIO[7:0] are 5V tolerant.

6. USB Timing Update: EOP Width

Issue: Section 16.4, AC Characteristics, update t106 in Table 16-12 with the following row:

Sym	Parameter	Min	Max	Unit	Notes	Figure
t106	EOP Width: Must accept as EOP	82		ns		16-15

7. Removal of DC Output Enhanced Mode Hublink Characteristics

Remove the following specification for Enhanced mode hublink. Enhanced mode is not supported on mobile platforms.

Issue: Remove V_{OL8} Enhanced Mode in Table 16-5:

Symbol	Parameter	Min	Max	Unit	I_{OL}/I_{OH}	Notes
V_{OL8}	Output Low Voltage		0.8	V	20mA	Enhanced Mode

Issue: Remove V_{OH8} Enhanced Mode in Table 16-5:

Symbol	Parameter	Min	Max	Unit	I_{OL}/I_{OH}	Notes
V_{OH8}	Output High Voltage	1.6		V	-1.5mA	Enhanced Mode

8. Vcc1_8 Max Power Consumption at S0

Issue: Replace max power consumption figure Vcc1_8 at S0 in Section 16-3, Table 16-1, *DC Characteristics*, with the following:

Power Plane	Maximum Power Consumption				
	S0	S1	S3	S4/S5	G3
Vcc1_8	**550 mA**	20 mA	N/A	N/A	N/A

9. V5REF_Sus Connectivity

Issue: In Section 2.19, Table 2-19, Power and Ground, add the following note in V5REF_Sus[2:1] description:

Note: See Platform Design Guide for V5REF_Sus connectivity.

10. SLP_S1# Power State at S3-S5

Issue: In Section 3.4, Table 3-4, Power Plane and States for Output and I/O Signals, replace signal SLP_S1# states with the following:

Signal Name	Power Plane	During PCIRST# / RSMRST#	Immediately After PCIRST# / RSMRST#	C3/C4	S1	S3	S4/S5
Power Management							
SLP_S1#	Main I/O	High	High	High	Low	**Off**	**Off**

11. SLP_S1# and STP_PCI# are swapped in 'S0 to S5 to S0' Timing Diagram

Issue: In Figure 16-22, *S0 to S5 to S0 Timing*, swap the signal names SLP_S1# and STP_PCI#.

12. LAN_RST# is Inactive after VccLAN Supplies Active

Issue: Table 16-18, *Power Sequencing and Reset Signal Timings*, replace Symbol t175b parameter with:

"VccLAN supplies active to LAN_RST# *inactive*"

13. SUSCLK AC Timing Specification

Issue: Add the following timing parameters to Table *16-7.Clock Timings* for SUSCLK:

Sym	Parameter	Min	Max	Unit	Notes	Figure
Suspend Clock (SUSCLK)						
f_{susclk}	Operating Frequency	32		KHz		
t14	High Time	10		us	6	**16-1**
t15	Low Time	10		us	6	**16-1**

14. SUSCLK During PCIRST#

Issue: Table 3-4, *Power Plane and States for Output and I/O Signals*, incorrectly indicates that SUSCLK is "Low" during PCIRST#. SUSCLK is low when RSMRST# is asserted but will be "Running" during PCIRST# assertion.

15. USB PORTSC Register

Issue: In Section 11.2.7 PORTSC[0, 1] - *Port Status and Control Register*, bit 9 **Port Reset** is R/W not R/O.

16. TCO Registers

Issue: TCOBase IO locations are incorrect for the following registers:

- Section 9.9.2: TCOBase+00h is TCO_RLD (not TCO1_RLD) and the default value is 00h (not 0000h)
- Section 9.9.3: TCOBase+01h is TCO_TMR (not TCO1_TMR) and the default value is 04h (not 0004h). Description incorrectly states "Value of 0-3h will be ignored.." where actually values of 0-1h will be ignored
- Section 9.9.4: TCOBase+02h is TCO_DAT_IN (not TCO1_DAT_IN) and the default is 00h (not 0000h). The description also incorrectly refers to "OS TCO_SMI" and "TCO_STS" which should be "SW_TCO_SMI" and "TCO1_STS"
- Section 9.9.5: TCOBase+03h is TCO_DAT_OUT (not TCO1_DAT_OUT) and the default value is 00h (not 0000h)

17. Generic Decode Range 2 Register Description Change

Issue: The description in Section 9.1.32 for the Generic I/O Decode Range Base Address should read the following:

"This address is aligned on a 16-byte boundary and must have address lines 31:16 as 0."